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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. : 10/628,906 Confirmation No.: 7434  
Applicant : Alan Marshall  
Filing Date : July 28, 2003  
Title : Methods and Systems for Reducing Leakage Current in Semiconductor Circuits  
Group Art Unit : 2816  
Examiner : My Trang Ton  
Docket No. : 703567.4001  
Customer No. : 34313

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUBMISSION OF CORRECTED FORMAL DRAWINGS**

Applicant hereby submits corrected formal drawing (13 sheets with 18 figures) for the above-referenced application. If there are any questions regarding these drawings, please call the undersigned. The Commissioner is authorized to charge any fee which may be required in connection with this Submission of Formal Drawings to deposit account No. 15-0665.

Respectfully submitted,  
ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: September 13, 2005

By: Donald Daybell  
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**CERTIFICATE OF MAILING**  
37 CFR §1.8

I hereby certify, pursuant to 37 CFR §1.8, that I have reasonable basis to expect that this paper or fee (along with any referred to as being attached or enclosed) would be mailed or transmitted on or before the date indicated with the United States Postal Service with sufficient postage as first class mail on the date shown below in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Dated: September 13, 2005

Sally Hartwell  
Sally Hartwell